

N-channel 1200 V, 0.62 Ω typ., 12 A MDmesh™ K5 Power MOSFETs in TO-220FP and TO-3PF packages

Datasheet - production data

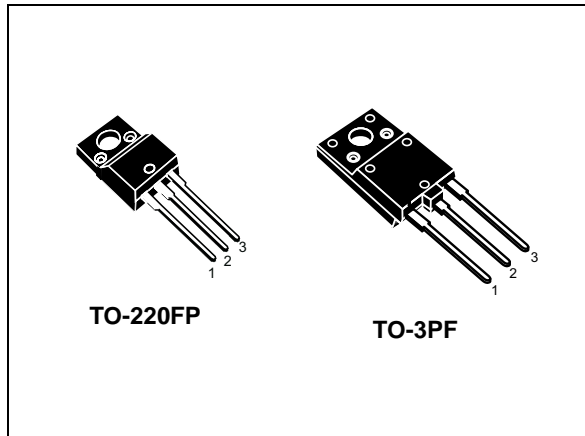
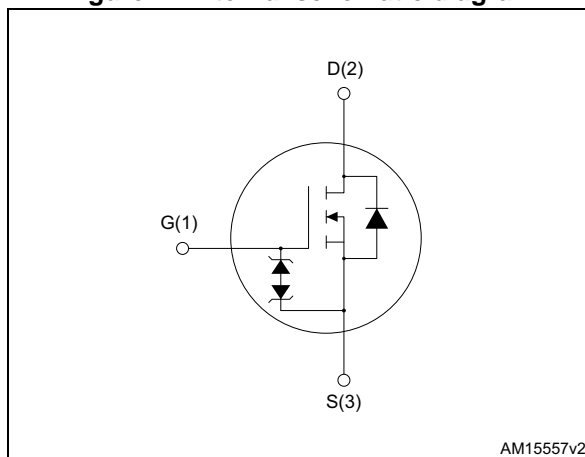


Figure 1. Internal schematic diagram



Features

| Order code | V_{DS} | $R_{DS(on)}$ max. | I_D | P_{TOT} |
|--------------|----------|-------------------|-------|-----------|
| STF12N120K5 | 1200 V | 0.69 Ω | 12 A | 40 W |
| STFW12N120K5 | | | | 63 W |

- Industry's lowest $R_{DS(on)}$ x area
- Industry's best figure of merit (FoM)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These very high voltage N-channel Power MOSFETs are designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1. Device summary

| Order code | Marking | Packages | Packing |
|--------------|----------|----------|---------|
| STF12N120K5 | 12N120K5 | TO-220FP | Tube |
| STFW12N120K5 | | TO-3PF | |

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1 Electrical ratings

Table 2. Absolute maximum ratings

| Symbol | Parameter | Value | | Unit |
|--------------------|---|-------------|--------|------|
| | | TO-220FP | TO-3PF | |
| V_{GS} | Gate-source voltage | ± 30 | | V |
| I_D | Drain current at $T_C = 25\text{ °C}$ | 12 | | A |
| I_D | Drain current at $T_C = 100\text{ °C}$ | 7.6 | | A |
| $I_{DM}^{(1)}$ | Drain current (pulsed) | 48 | | A |
| P_{TOT} | Total dissipation at $T_C = 25\text{ °C}$ | 40 | 63 | W |
| V_{ISO} | Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$, $T_C = 25\text{ °C}$) | 2500 | 3500 | V |
| $I_{AR}^{(2)}$ | Max current during repetitive or single pulse avalanche | 4 | | A |
| $E_{AS}^{(3)}$ | Single pulse avalanche energy | 215 | | mJ |
| $dv/dt^{(4)}$ | Peak diode recovery voltage slope | 4.5 | | V/ns |
| $dv/dt^{(5)}$ | MOSFET dv/dt ruggedness | 50 | | V/ns |
| T_j T_{stg} | Operating junction temperature Storage temperature | - 55 to 150 | | °C |

1. Pulse width limited by safe operating area.
2. Pulse width limited by T_{Jmax} .
3. Starting $T_J = 25\text{ °C}$, $I_D = I_{AS}$, $V_{DD} = 50\text{ V}$
4. $I_{SD} \leq 12\text{ A}$, $di/dt \leq 100\text{ A}/\mu\text{s}$, $V_{Peak} \leq V_{(BR)DSS}$
5. $V_{DS} \leq 960\text{ V}$

Table 3. Thermal data

| Symbol | Parameter | Value | | Unit |
|----------------|--------------------------------------|----------|--------|------|
| | | TO-220FP | TO-3PF | |
| $R_{thj-case}$ | Thermal resistance junction-case max | 3.1 | 1.98 | °C/W |
| $R_{thj-amb}$ | Thermal resistance junction-amb max | 62.5 | 50 | °C/W |

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|--|--|------|------|----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage, ($V_{GS} = 0$) | $I_D = 1\text{ mA}$ | 1200 | | | V |
| I_{DSS} | Zero gate voltage drain current ($V_{GS} = 0$) | $V_{DS} = 1200\text{ V}$ | | | 1 | μA |
| | | $V_{DS} = 1200\text{ V}$, $T_C = 125\text{ °C}$ | | | 50 | μA |
| I_{GSS} | Gate body leakage current ($V_{DS} = 0$) | $V_{GS} = \pm 20\text{ V}$ | | | ± 10 | μA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}$, $I_D = 100\text{ }\mu\text{A}$ | 3 | 4 | 5 | V |
| $R_{DS(on)}$ | Static drain-source on resistance | $V_{GS} = 10\text{ V}$, $I_D = 6\text{ A}$ | | 0.62 | 0.69 | Ω |

Table 5. Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-------------------|--|--|------|------|------|----------|
| C_{iss} | Input capacitance | $V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$ | - | 1370 | - | pF |
| C_{oss} | Output capacitance | | - | 110 | - | pF |
| C_{rss} | Reverse transfer capacitance | | - | 0.6 | - | pF |
| $C_{o(tr)}^{(1)}$ | Equivalent capacitance, time-related | $V_{GS} = 0$, $V_{DS} = 0\text{ to }960\text{ V}$ | - | 128 | - | pF |
| $C_{o(er)}^{(2)}$ | Equivalent capacitance, energy-related | | - | 42 | - | pF |
| R_G | Intrinsic gate resistance | $f = 1\text{ MHz}$, $I_D = 0$ | - | 3.5 | - | Ω |
| Q_g | Total gate charge | $V_{DD} = 960\text{ V}$, $I_D = 6\text{ A}$ $V_{GS} = 10\text{ V}$ (see Figure 18) | - | 44.2 | - | nC |
| Q_{gs} | Gate-source charge | | - | 7.3 | - | nC |
| Q_{gd} | Gate-drain charge | | - | 30 | - | nC |

1. Time-related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. Energy-related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------|---------------------|--|------|------|------|------|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 600\text{ V}$, $I_D = 6\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 20) | - | 23 | - | ns |
| t_r | Rise time | | - | 11 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 68.5 | - | ns |
| t_f | Fall time | | - | 18.5 | - | ns |

Table 7. Source drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------|-------------------------------|--|------|------|------|---------------|
| I_{SD} | Source-drain current | | - | | 12 | A |
| I_{SDM} | Source-drain current (pulsed) | | - | | 48 | A |
| $V_{SD}^{(1)}$ | Forward on voltage | $I_{SD} = 12\text{ A}$, $V_{GS} = 0$ | - | | 1.5 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 12\text{ A}$, $V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, (see Figure 19) | - | 630 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 12.6 | | μC |
| I_{RRM} | Reverse recovery current | | - | 40 | | A |
| t_{rr} | Reverse recovery time | $I_{SD} = 12\text{ A}$, $V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 19) | - | 892 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 15.6 | | μC |
| I_{RRM} | Reverse recovery current | | - | 35 | | A |

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 8. Gate-source Zener diode

| Symbol | Parameter | Test conditions | Min | Typ. | Max. | Unit |
|---------------|-------------------------------|--|-----|------|------|------|
| $V_{(BR)GSO}$ | Gate-source breakdown voltage | $I_{GS} = \pm 1\text{ mA}$, $I_D = 0$ | 30 | - | | V |

The built-in back-to-back Zener diodes have been specifically designed to enhance the ESD capability of the device. The Zener voltage is appropriate for efficient and cost-effective intervention to protect the device integrity. These integrated Zener diodes thus eliminate the need for external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220FP

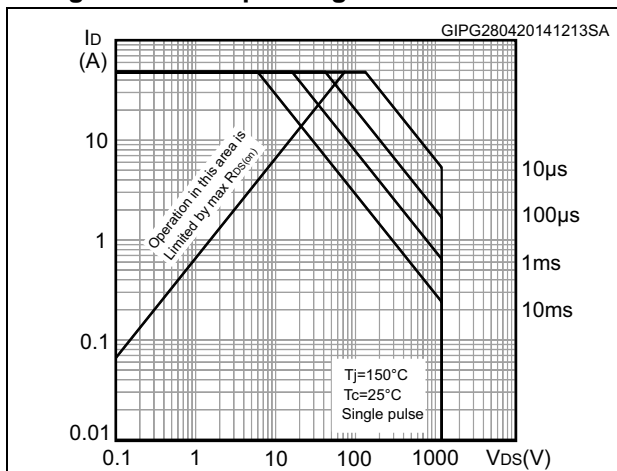


Figure 3. Thermal impedance for TO-220FP

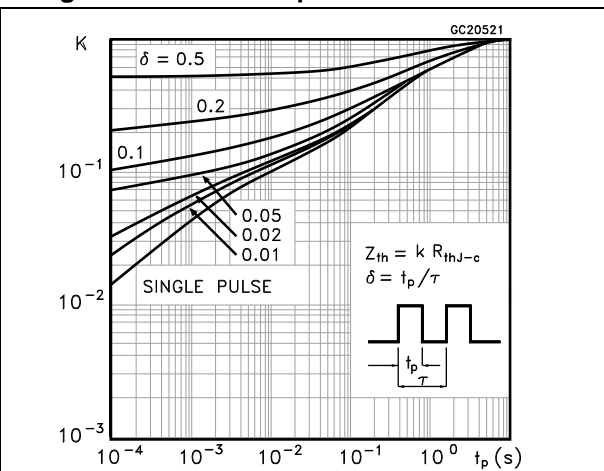


Figure 4. Safe operating area for TO-3PF

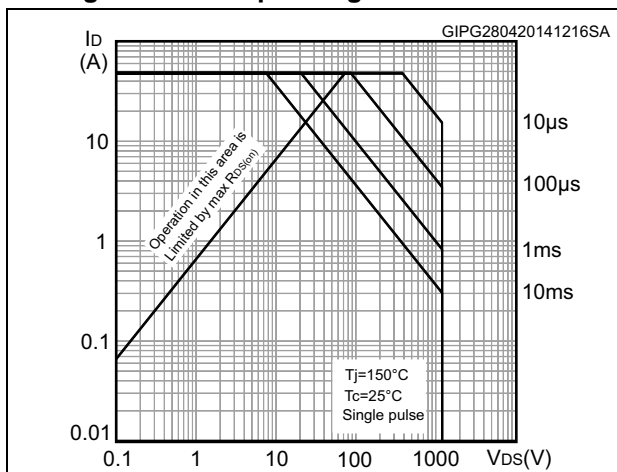


Figure 5. Thermal impedance for TO-3PF

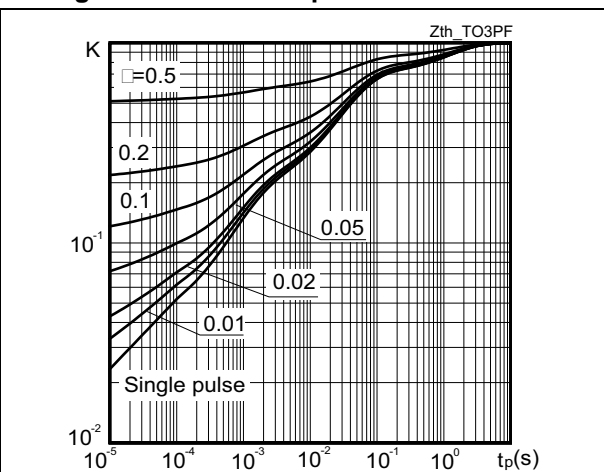


Figure 6. Output characteristics

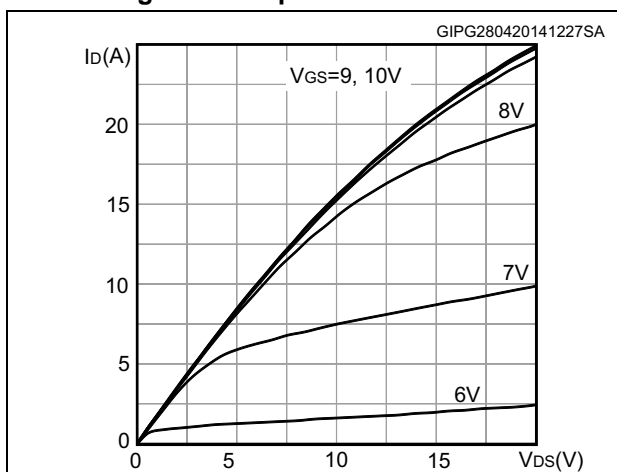


Figure 7. Transfer characteristics

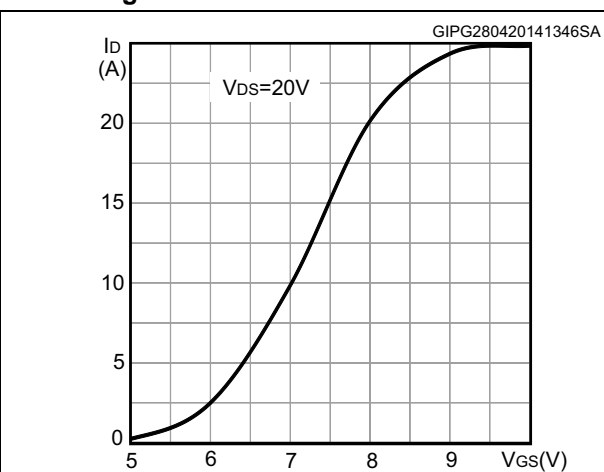


Figure 8. Gate charge vs gate-source voltage

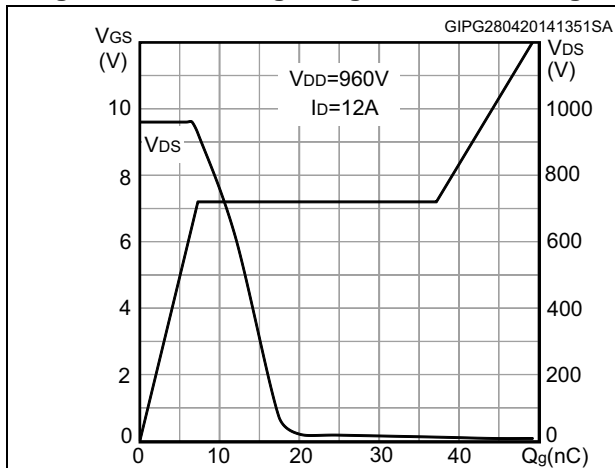


Figure 9. Static drain-source on-resistance

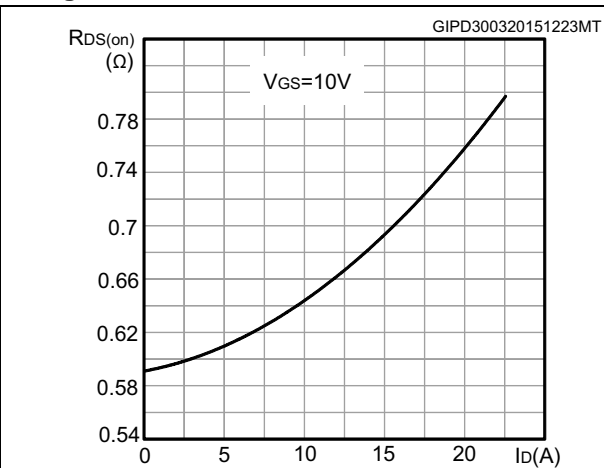


Figure 10. Capacitance variations

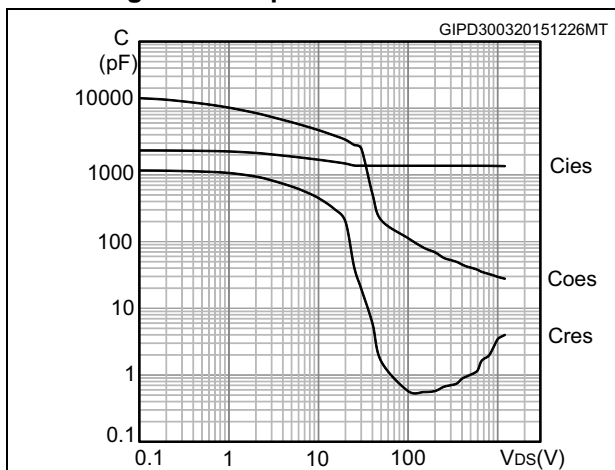


Figure 11. Output capacitance stored energy

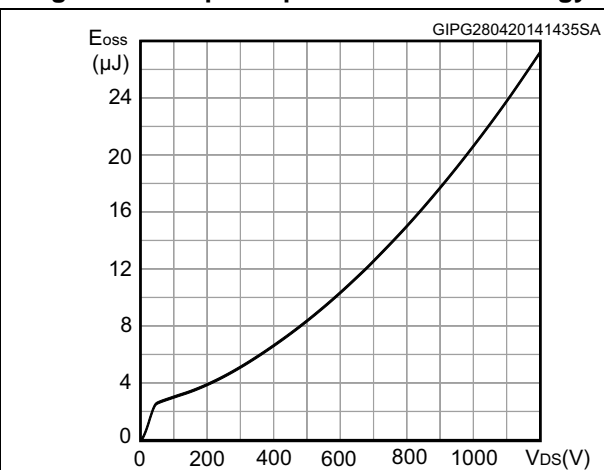


Figure 12. Normalized gate threshold voltage vs temperature

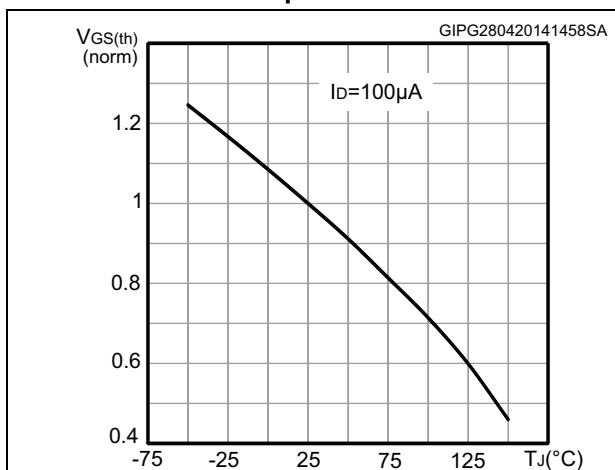


Figure 13. Normalized on-resistance vs temperature

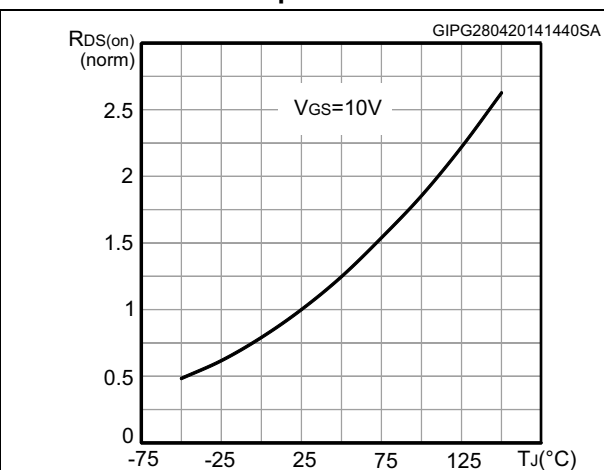


Figure 14. Normalized $V_{(BR)DSS}$ vs temperature

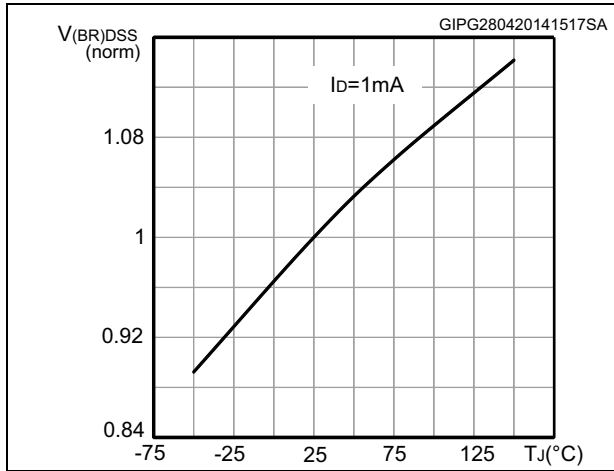


Figure 15. Source-drain diode forward characteristics

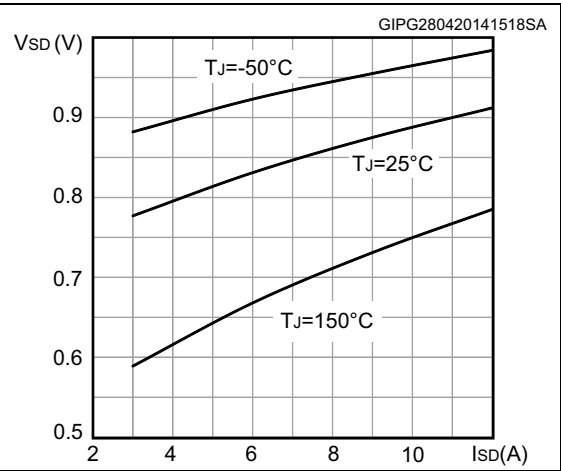
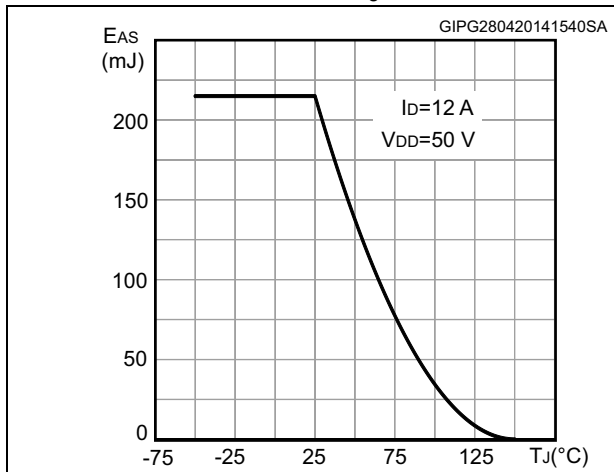


Figure 16. Maximum avalanche energy vs starting T_J



3 Test circuits

Figure 17. Switching time test circuit for resistive load

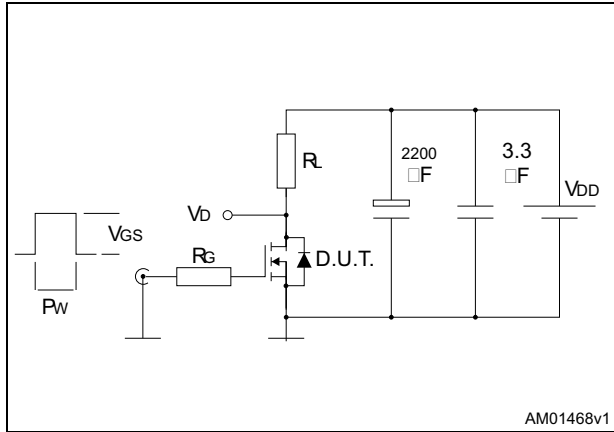


Figure 18. Gate charge test circuit

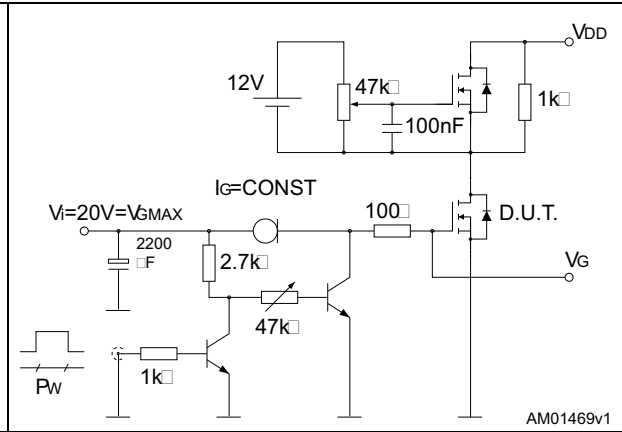


Figure 19. Test circuit for inductive load switching and diode recovery times

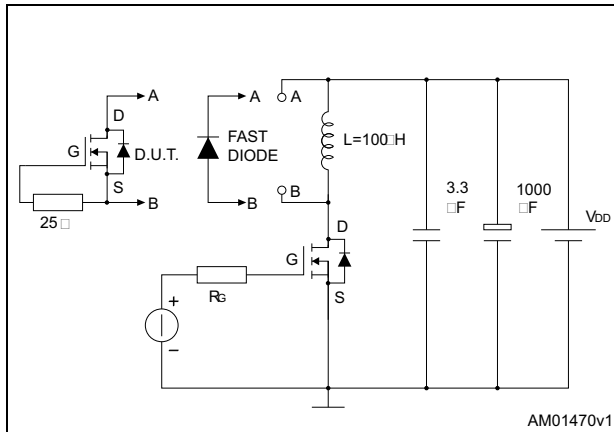


Figure 20. Unclamped inductive load test circuit

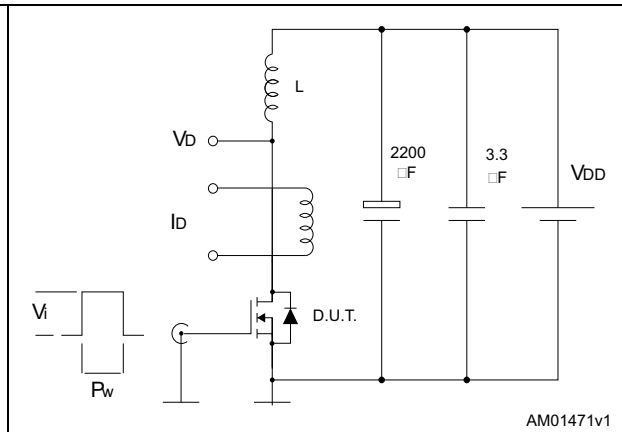


Figure 21. Unclamped inductive waveform

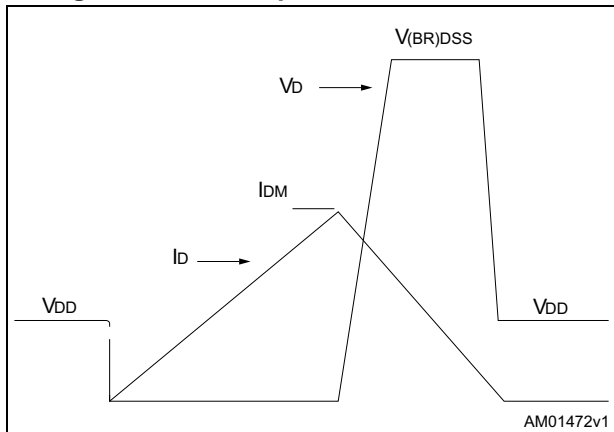
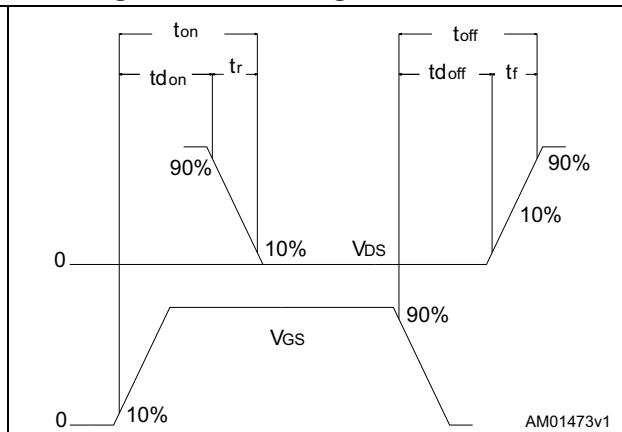


Figure 22. Switching time waveform

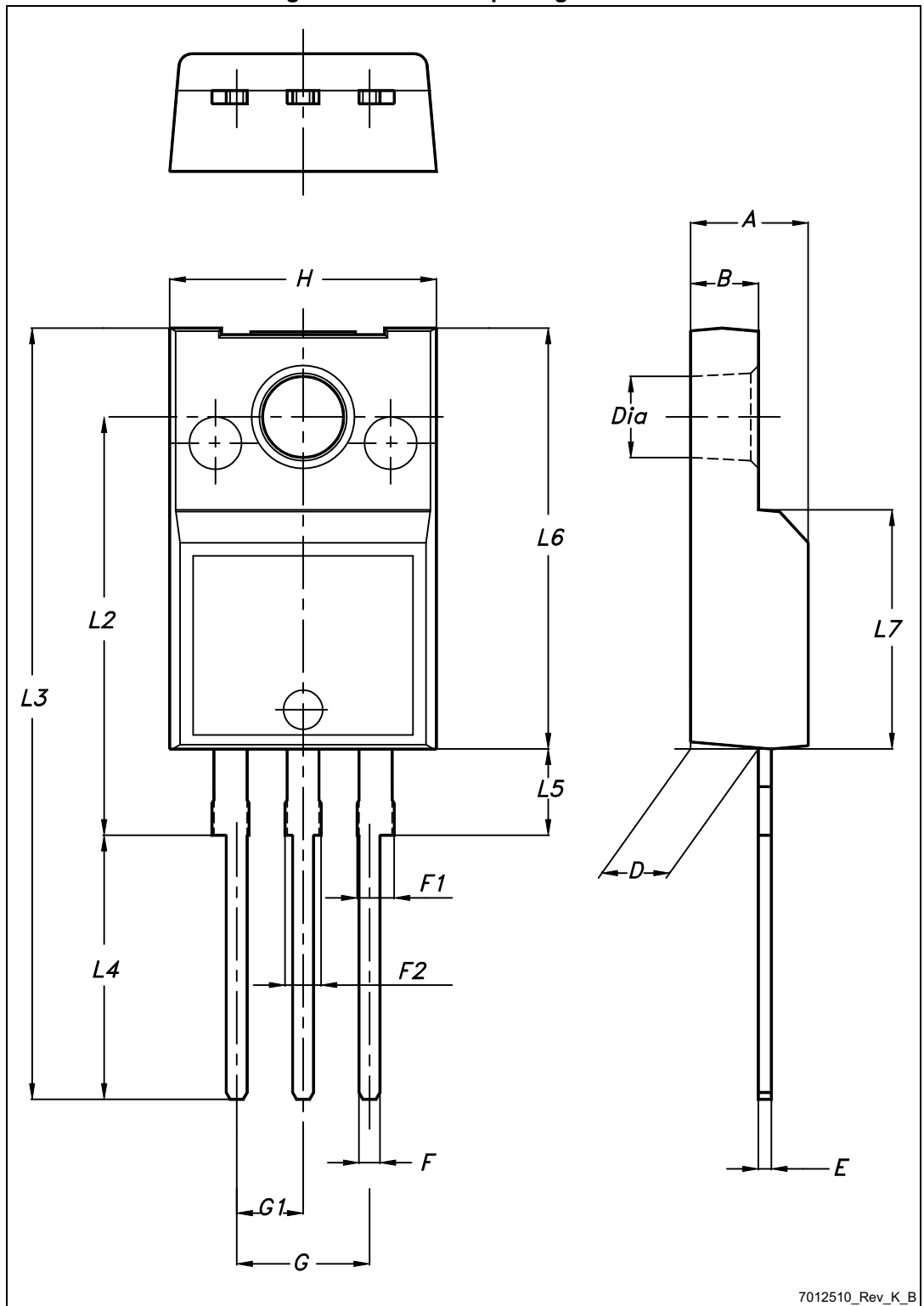


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 TO-220FP, package outline

Figure 23. TO-220FP package outline



7012510_Rev_K_B

Table 9. TO-220FP mechanical data

| Dim. | mm | | |
|------|------|------|------|
| | Min. | Typ. | Max. |
| A | 4.4 | | 4.6 |
| B | 2.5 | | 2.7 |
| D | 2.5 | | 2.75 |
| E | 0.45 | | 0.7 |
| F | 0.75 | | 1 |
| F1 | 1.15 | | 1.70 |
| F2 | 1.15 | | 1.70 |
| G | 4.95 | | 5.2 |
| G1 | 2.4 | | 2.7 |
| H | 10 | | 10.4 |
| L2 | | 16 | |
| L3 | 28.6 | | 30.6 |
| L4 | 9.8 | | 10.6 |
| L5 | 2.9 | | 3.6 |
| L6 | 15.9 | | 16.4 |
| L7 | 9 | | 9.3 |
| Ø | 3 | | 3.2 |

4.2 TO-3PF, package outline

Figure 24. TO-3PF package outline

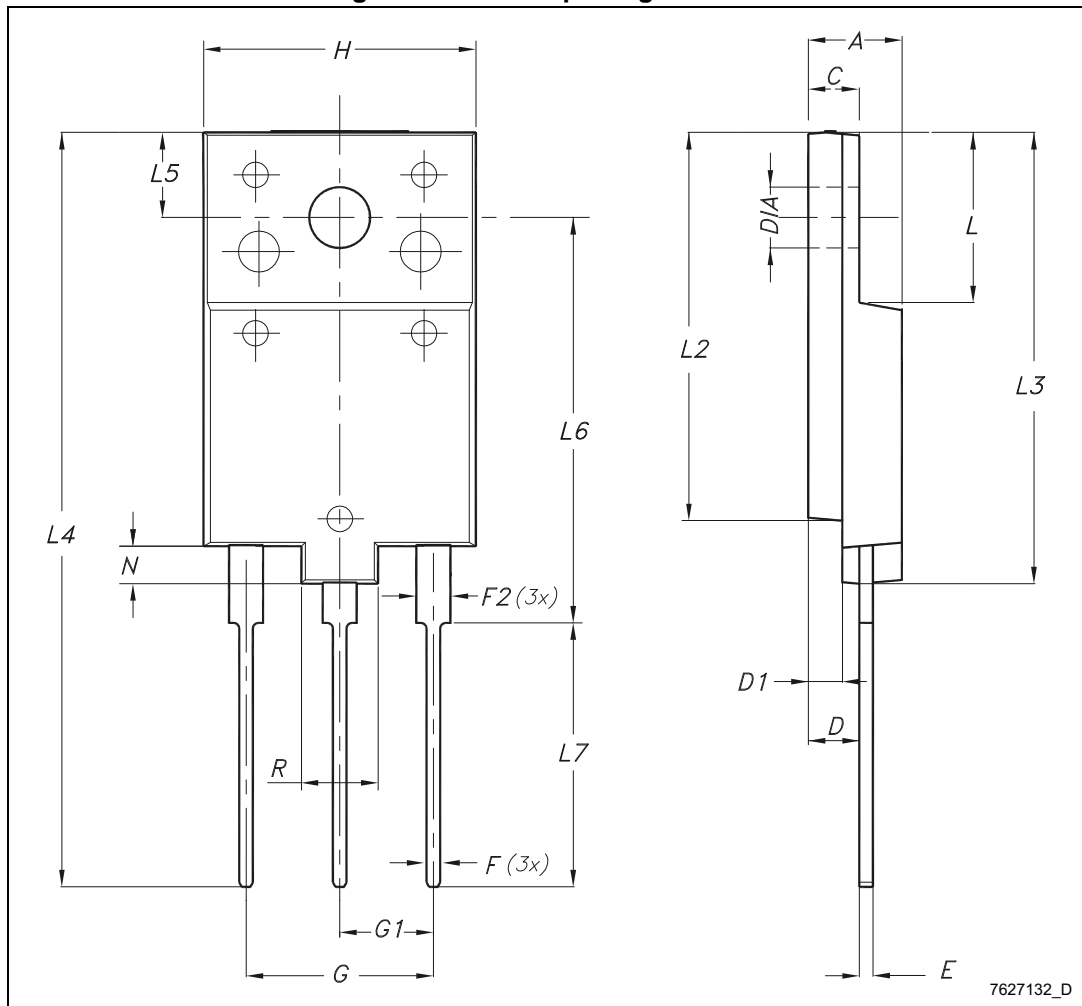


Table 10. TO-3PF mechanical data

| Dim. | mm | | |
|------|-------|------|-------|
| | Min. | Typ. | Max. |
| A | 5.30 | | 5.70 |
| C | 2.80 | | 3.20 |
| D | 3.10 | | 3.50 |
| D1 | 1.80 | | 2.20 |
| E | 0.80 | | 1.10 |
| F | 0.65 | | 0.95 |
| F2 | 1.80 | | 2.20 |
| G | 10.30 | | 11.50 |
| G1 | | 5.45 | |
| H | 15.30 | | 15.70 |
| L | 9.80 | 10 | 10.20 |
| L2 | 22.80 | | 23.20 |
| L3 | 26.30 | | 26.70 |
| L4 | 43.20 | | 44.40 |
| L5 | 4.30 | | 4.70 |
| L6 | 24.30 | | 24.70 |
| L7 | 14.60 | | 15 |
| N | 1.80 | | 2.20 |
| R | 3.80 | | 4.20 |
| ∅ | 3.40 | | 3.80 |

5 Revision history

Table 11. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 22-May-2014 | 1 | First release. Part number (STFW12N120K5) previously included in datasheet DocID022133 |
| 11-May-2015 | 2 | Updated title, features and description. Updated Table 4.: On/off states and Table 5.: Dynamic . Updated Figure 9.: Static drain-source on-resistance and Figure 10.: Capacitance variations Minor text changes. |

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