Freescale Semiconductor
Technical Data

Document Number: MRF7S15100H
Rev. 0, 7/2008

RoHS

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

MRF7S15100HR3
MRF7S15100HSR3

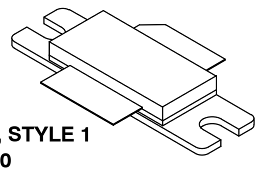
Designed for CDMA base station applications with frequencies from 1470 to 1510 MHz. Suitable for TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB and Class C for PCN-PCS/cellular radio and WLL applications.

- Typical Single-Carrier W-CDMA Performance: V_{DD} = 28 Volts, I_{DQ} = 600 mA, P_{out} = 23 Watts Avg., f = 1507.5 MHz, 3GPP Test Model 1, 64 DPCH with 50% Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.
  Power Gain — 19.5 dB
  Drain Efficiency — 32%
  Device Output Signal PAR — 6.2 dB @ 0.01% Probability on CCDF
  ACPR @ 5 MHz Offset — -38 dBc in 3.84 MHz Channel Bandwidth
- Capable of Handling 10:1 VSWR, @ 32 Vdc, 1490 MHz, 100 Watts CW Output Power
- Typical P_{out} @ 1 dB Compression Point ≃ 100 Watts CW

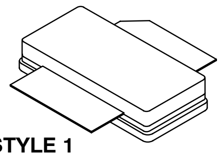
Features

- 100% PAR Tested for Guaranteed Output Power Capability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Optimized for Doherty Applications
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.

1510 MHz, 23 W AVG., 28 V
SINGLE W-CDMA
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465-06, STYLE 1
NI-780
MRF7S1500HR3



CASE 465A-06, STYLE 1
NI-780S
MRF7S1500HSR3

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1)	T_J	225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 55 W CW Case Temperature 77°C, 23 W CW	$R_{\theta JC}$	 0.65 0.74	°C/W

1. Continuous use at maximum temperature will affect MTTF.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

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Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	IC (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Electrical Characteristics (T_C = 25°C unless otherwise noted)

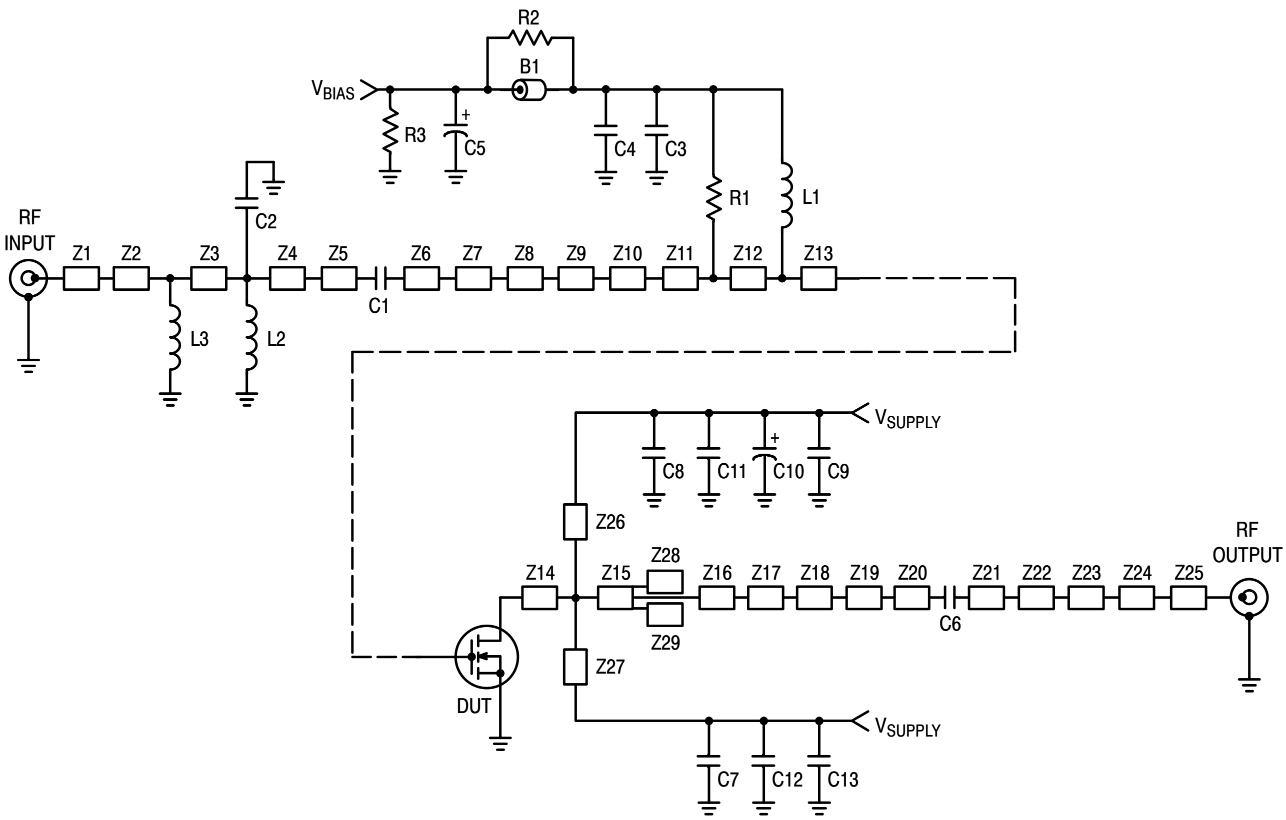
Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DD} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 174 μAdc)	$V_{GS(th)}$	1.2	2	2.7	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_D = 600 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	2	2.7	3.5	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1.74 Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc
Dynamic Characteristics (1)					
Reverse Transfer Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	0.6	—	pF
Output Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	300	—	pF
Input Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc ± 30 mV(rms)ac @ 1 MHz)	C_{iss}	—	176	—	pF
Functional Tests (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 600 mA, P_{out} = 23 W Avg., f = 1507.5 MHz, Single-Carrier W-CDMA, 3GPP Test Model 1, 64 DPCH, 50% Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	18	19.5	21	dB
Drain Efficiency	η_D	30	32	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	5.9	6.2	—	dB
Adjacent Channel Power Ratio	ACPR	—	-38	-35	dBc
Input Return Loss	IRL	—	-15	-8	dB

1. Part internally matched both on input and output.

(continued)

Table 4. Electrical Characteristics (T_C = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 600 mA, 1470-1510 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	100	—	W
IMD Symmetry @ 90 W PEP, P_{out} where IMD Third Order Intermodulation ≅ 30 dBc (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands > 2 dB)	IMD_{sym}	—	40	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	70	—	MHz
Gain Flatness in 40 MHz Bandwidth @ P_{out} = 23 W Avg.	G_F	—	0.2	—	dB
Average Deviation from Linear Phase in 40 MHz Bandwidth @ P_{out} = 100 W CW	Φ	—	4.5	—	°
Average Group Delay @ P_{out} = 100 W CW, f = 1490 MHz	Delay	—	1.9	—	ns
Part-to-Part Insertion Phase Variation @ P_{out} = 100 W CW, f = 1490 MHz, Six Sigma Window	ΔΦ	—	23	—	°
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.010	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	ΔP1dB	—	0.007	—	W/°C



Z1	0.084″ x 0.078″ Microstrip	Z15	1.330″ x 0.538″ Microstrip
Z2	0.149″ x 0.153″ Microstrip	Z16	0.270″ x 0.280″ Microstrip
Z3	0.149″ x 0.303″ Microstrip	Z17	0.187″ x 0.150″ Microstrip
Z4	0.149″ x 0.065″ Microstrip	Z18	0.084″ x 0.042″ Microstrip
Z5	0.084″ x 0.146″ Microstrip	Z19	0.184″ x 0.292″ Microstrip
Z6	0.084″ x 0.104″ Microstrip	Z20	0.084″ x 0.066″ Microstrip
Z7	0.218″ x 0.080″ Microstrip	Z21	0.886″ x 0.194″ Microstrip
Z8	0.084″ x 0.206″ Microstrip	Z22	0.300″ x 0.084″ Microstrip
Z9	0.224″ x 0.085″ Microstrip	Z23	0.084″ x 0.215″ Microstrip
Z10	0.084″ x 0.369″ Microstrip	Z24	0.221″ x 0.075″ Microstrip
Z11	1.288″ x 0.206″ Microstrip	Z25	0.084″ x 0.175″ Microstrip
Z12	1.288″ x 0.144″ Microstrip	Z26, Z27	0.200″ x 0.525″ Microstrip
Z13	1.288″ x 0.369″ Microstrip	Z28, Z29	0.235″ x 0.102″ Microstrip
Z14	1.330″ x 0.112″ Microstrip	PCB	Arlon CuClad 250GX-0300-55-22, 0.030″, ε_r = 2.55

Figure 1. MRF7S15100HR3(HSR3) Test Circuit Schematic

Table 5. MRF7S15100HR3(HSR3) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
B1	Short Ferrite Bead	2743019447	Fair-Rite
C1, C6, C7, C8	15 pF Chip Capacitors	ATC100B150JT500XT	ATC
C2	0.5 pF Chip Capacitor	ATC100B0R5BT500XT	ATC
C3	10 pF Chip Capacitor	ATC100B100JT500XT	ATC
C4, C9, C13	6.8 μF, 50 V Chip Capacitors	C4532JB1H685MT	TDK
C5, C10	100 μF, 50 V Electrolytic Capacitors	222215371101	Vishay
C11, C12	2.2 μF, 50 V Chip Capacitors	C3225JB2A225MT	TDK
L1, L2, L3	7.15 nH Inductors	1606-TLC	Coilcraft
R1, R2	100 Ω, 1/4 W Chip Resistors	CRCW12061000FKEA	Vishay
R3	10 KΩ, 1/4 W Chip Resistor	CRCW12061002FKEA	Vishay

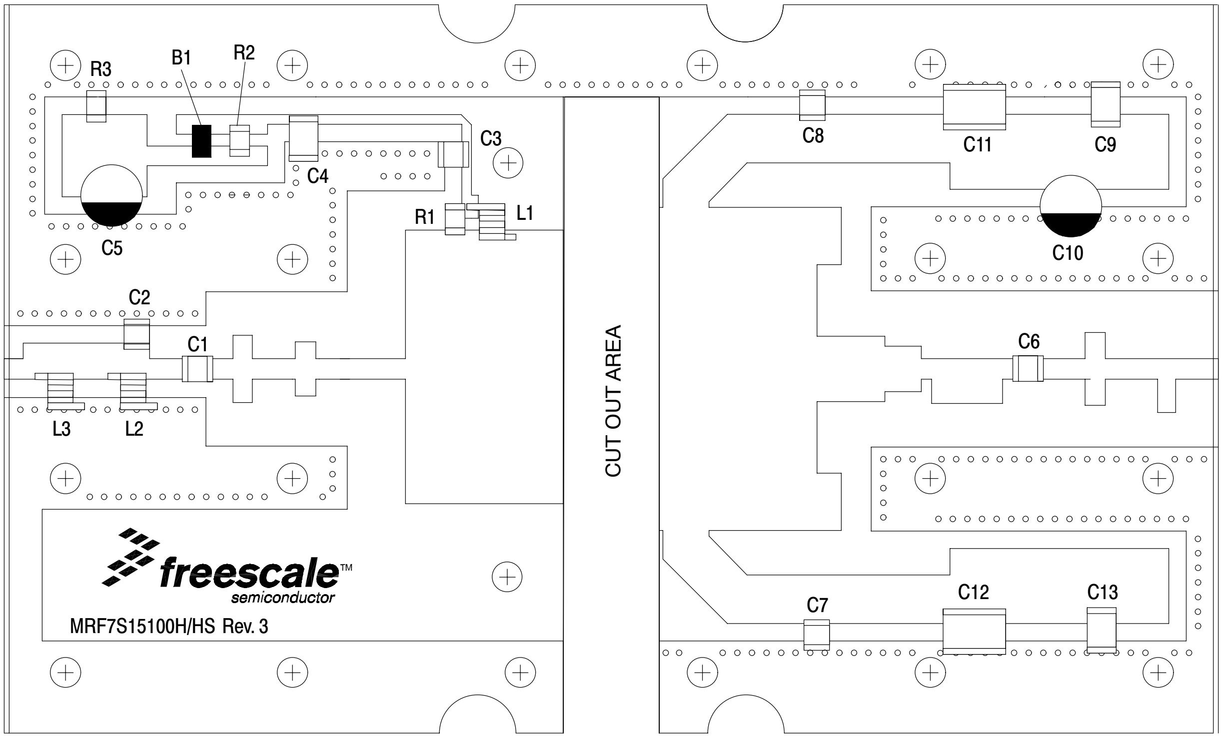


Figure 2. MRF7S15100HR3(HSR3) Test Circuit Component Layout

TYPICAL CHARACTERISTICS

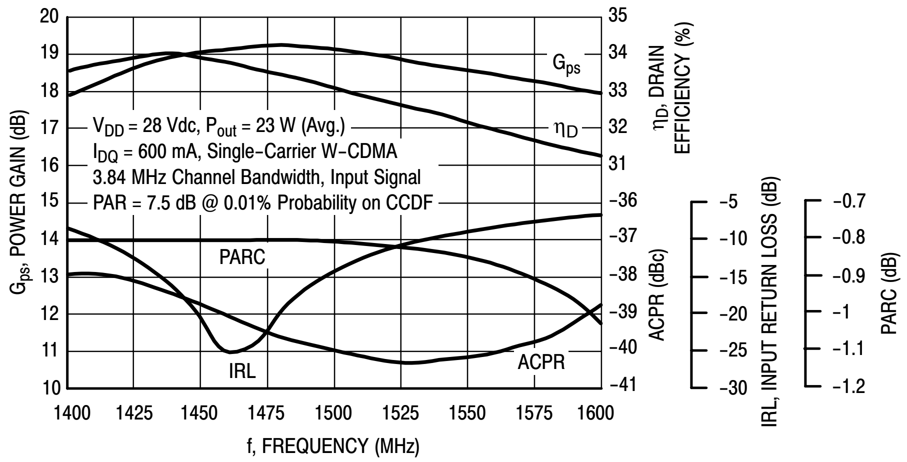


Figure 3. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 23 Watts Avg.

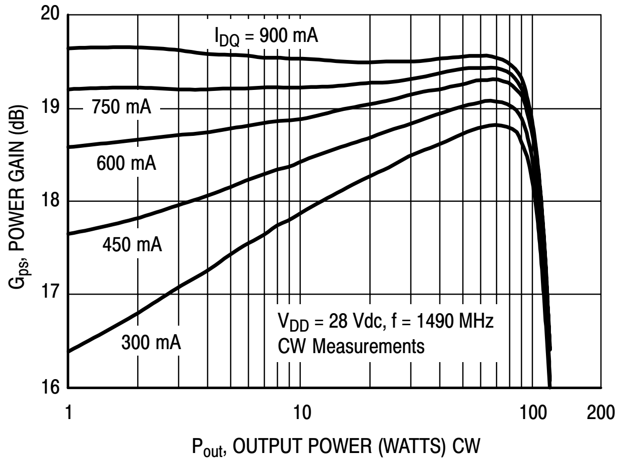


Figure 4. CW Power Gain versus Output Power

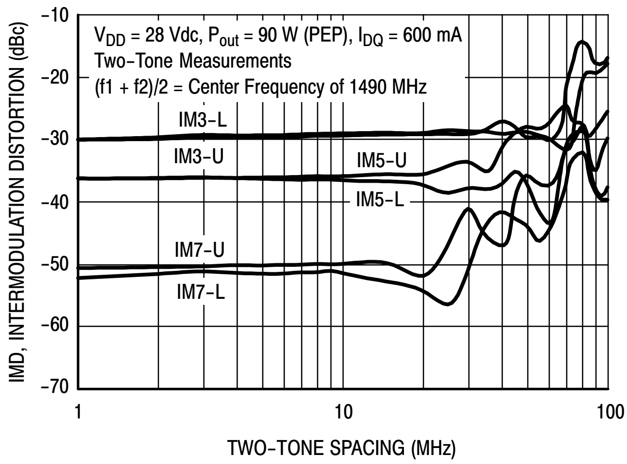


Figure 5. Intermodulation Distortion Products versus Tone Spacing

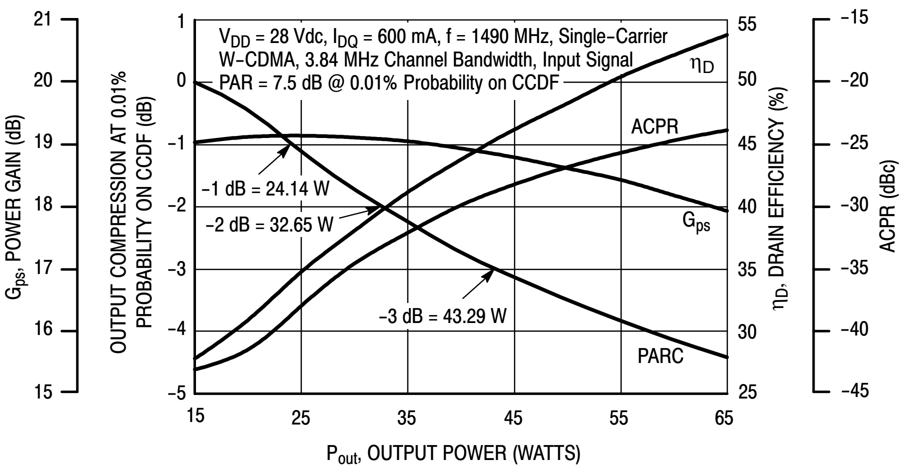


Figure 6. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

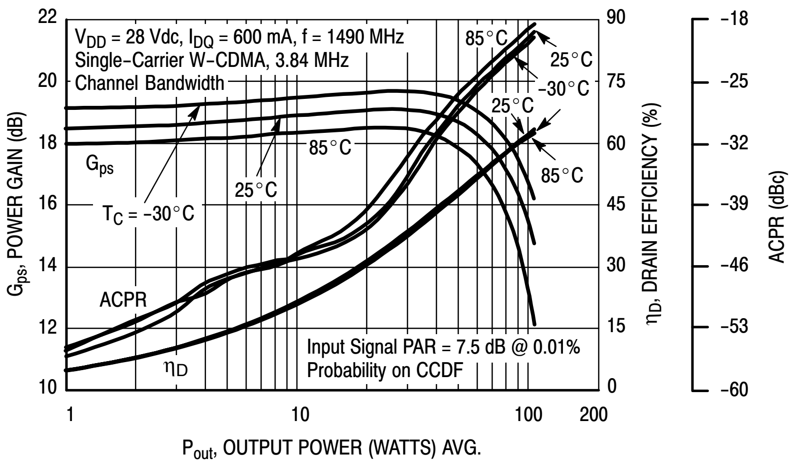


Figure 7. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

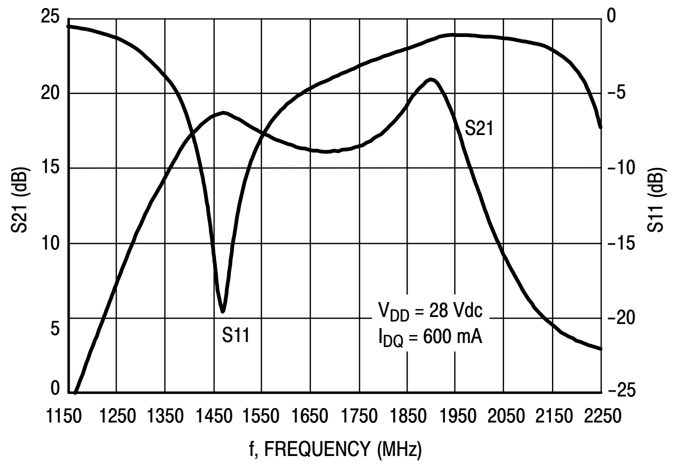


Figure 8. Broadband Frequency Response

W-CDMA TEST SIGNAL

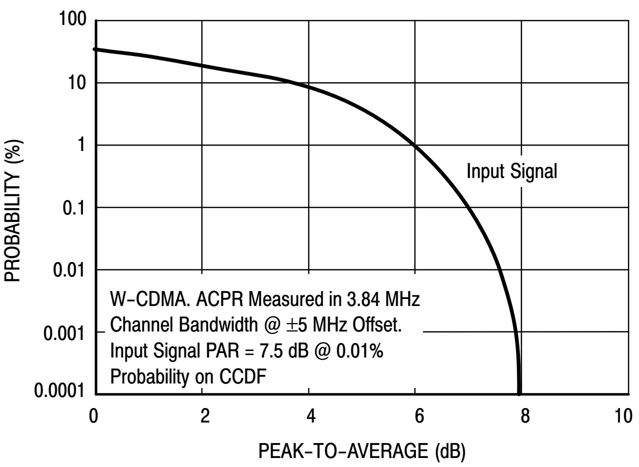


Figure 9. CCDF W-CDMA 3GPP, Test Model 1, 64 DPCH, 50% Clipping, Single-Carrier Test Signal

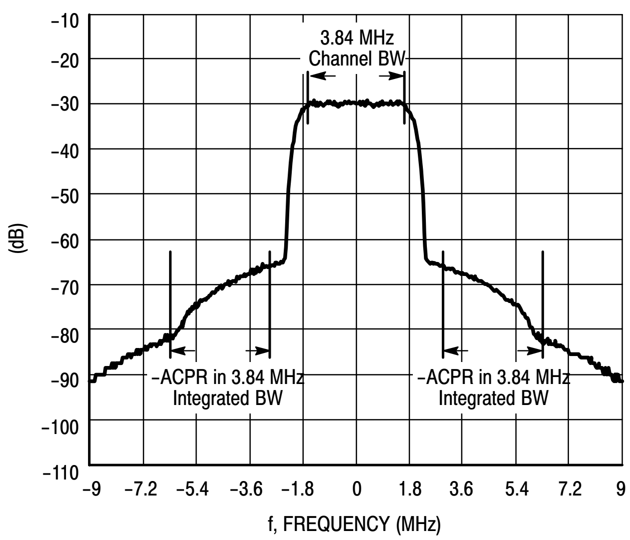
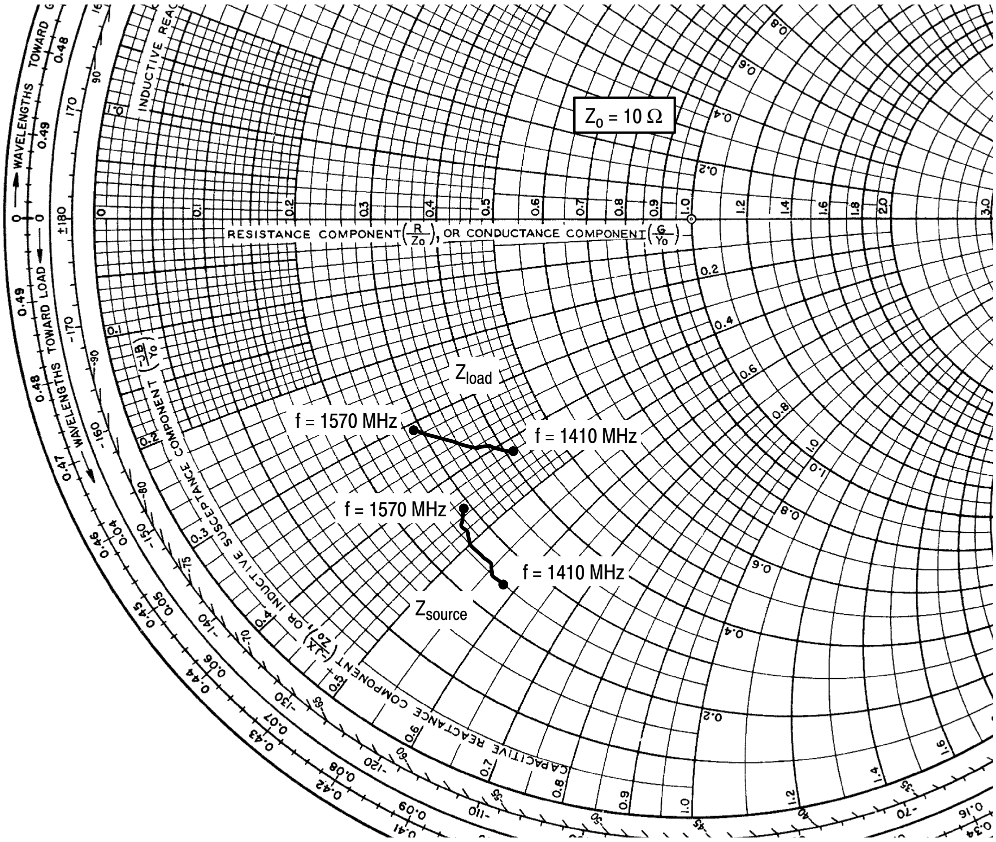


Figure 10. Single-Carrier W-CDMA Spectrum



V_{DD} = 28 Vdc, I_{DQ} = 600 mA, P_{out} = 23 W Avg.

f MHz	Z_{source} Ω	Z_{load} Ω
1410	2.51 - j5.82	4.12 - j4.20
1430	2.53 - j5.58	3.95 - j4.07
1450	2.55 - j5.36	3.78 - j3.94
1470	2.58 - j5.15	3.61 - j3.80
1490	2.62 - j4.97	3.45 - j3.65
1510	2.67 - j4.81	3.30 - j3.51
1530	2.73 - j4.68	3.15 - j3.37
1550	2.79 - j4.57	3.00 - j3.22
1570	2.85 - j4.49	2.87 - j3.06

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

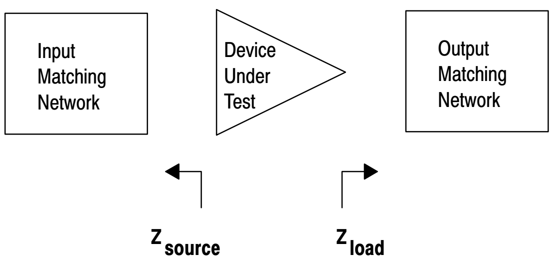
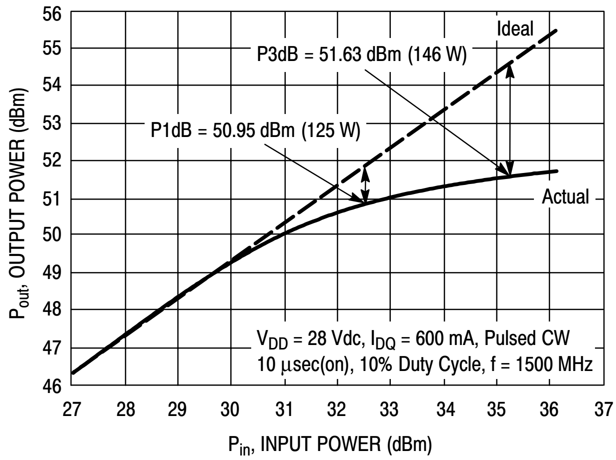


Figure 11. Series Equivalent Source and Load Impedance

ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS



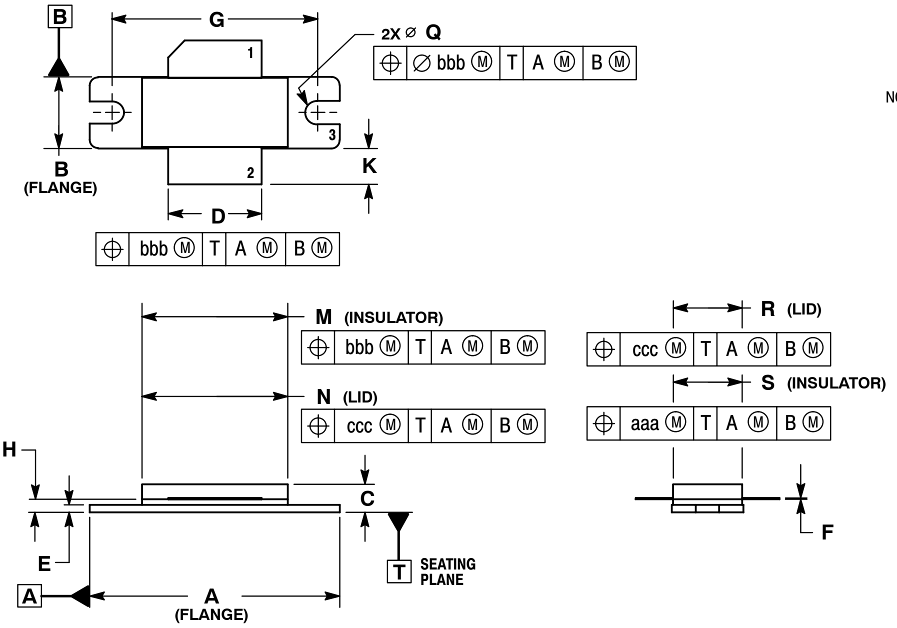
NOTE: Load Pull Test Fixture Tuned for Peak P1dB Output Power @ 28 V

Test Impedances per Compression Level

	Z_{source} Ω	Z_{load} Ω
P1dB	2.02 + j6.21	2.00 - j3.65

Figure 12. Pulsed CW Output Power versus Input Power @ 28 V

PACKAGE DIMENSIONS

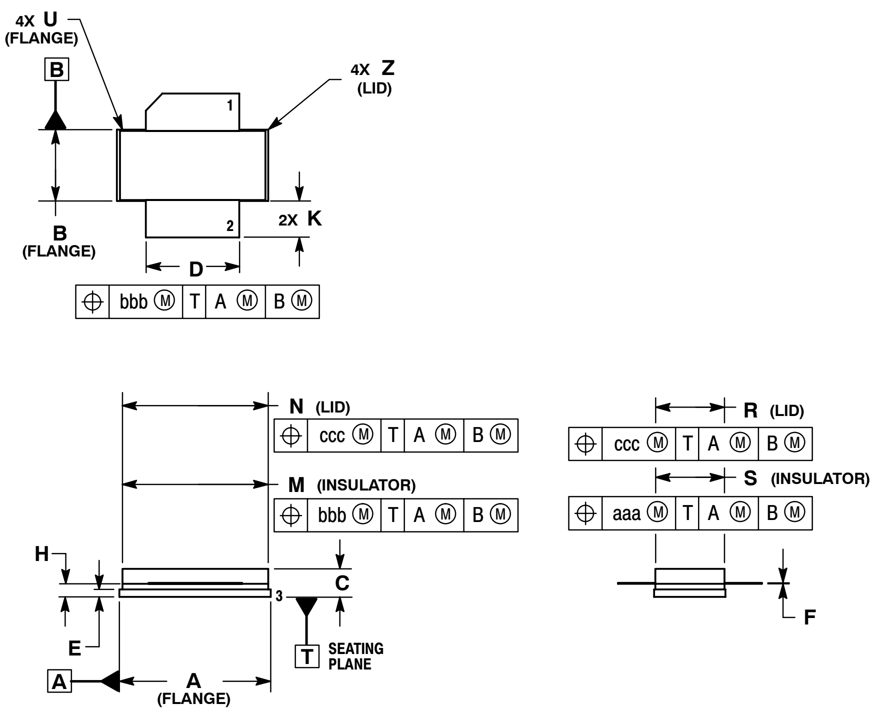


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M−1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.335	1.345	33.91	34.16
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.66	19.96
N	0.772	0.788	19.60	20.00
Q	∅.118	∅.138	∅3.00	∅3.51
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465-06
ISSUE G
NI-780
MRF7S15100HR3



NOTES:
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3. DELETED
4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.805	0.815	20.45	20.70
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.61	20.02
N	0.772	0.788	19.61	20.02
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
U	---	0.040	---	1.02
Z	---	0.030	---	0.76
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
5. SOURCE

CASE 465A-06
ISSUE H
NI-780S
MRF7S15100HSR3

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	July 2008	• Initial Release of Data Sheet

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Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
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Asia/Pacific:
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